(54) COMPOUND SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
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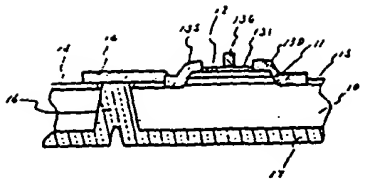
PURPOSE: To enable a viahole excellent in shape to be provided to a substrate from the rear side by a method wherein an etching-resistant thin film is provided between a source (or drain) pad electrode and a compound semiconductor layer when an InP substrate is etched.

CONSTITUTION: A buffer layer 11 and an N-type operating layer 12 are successively formed on the primary surface of a semi-insulating InP substrate 10, a source electrode 13S and a drain electrode 13D formed separate from each other by AuGe on the N-type operating layer 12, a gate insulating film 13I is provided onto a region sandwiched between the electrodes 13S and 13D, and a gate electrode 13G is formed on the gate insulating film 13I. A source pad electrode 14 electrically connected to the source electrode 13S is formed as led out from the electrode 13S. The pad electrode 14 is made to extend over a thin film 15 which is resistant to an etchant used for etching the InP substrate 10 to a viahole 15 and electrically connected to a back metal layer 17 through the viahole 16.



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⑭発明の名称　化合物半導体装置及びその製造方法

⑳特　願　平2−254310

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明　細　書

1．発明の名称

化合物半導体装置及びその製造方法

2．特許請求の範囲

（1）化合物半導体基板の一主面上に形成された動作層と、この動作層上に設けられたゲート電極と、このゲート電極を挟んで前記動作層上で対向するソース電極及びドレイン電極と、前記化合物半導体基板の裏面に形成された導体層と、前記ソース又はドレイン電極と電気的に接続されかつバイアホールを通して前記裏面導体層と電気的に接続されたソースパッド部又はドレインパッド部と、前記化合物半導体基板と前記ソースパッド部又はドレインパッド部との間に配置され、前記化合物半導体基板を蝕刻するエッチング手段に耐蝕性を有する薄膜層とより成る化合物半導体装置。

（以下余白）

（2）化合物半導体基板の一主面上に、ゲート電極と、このゲート電極を挟んで対向するソース電極及びドレイン電極とを形成する工程と、前記半導体基板を蝕刻するエッチング手段に耐蝕性を有する薄膜を形成する工程と、前記薄膜上及び前記半導体基板上に引出して設けられ、前記ソースもしくはドレイン電極と電気的に接続された各パッド部を形成する工程と、前記半導体基板の裏面側から該半導体基板をエッチングし、前記薄膜層に到達する貫通孔を形成する工程と、前記薄膜層をエッチングし前記ソース又はドレインパッド部に到達するバイアホールを形成する工程と、前記バイアホールを介して前記パッド部と電気的に接続された裏面導体層を形成する工程とを含むことを特徴とする化合物半導体装置の製造方法。

（3）化合物半導体基板がInPであることを特徴とする請求項（2）記載の化合物半導体装置の製造方法。

本発明は、上記の問題点を解消するためになされたもので、バイアホール構造を備えた良好な特性のＩｎＰ　ＦＥＴ、及びその製造方法を提供することを目的としている。

〔発明の構成〕

（課題を解決するための手段）

上記目的を達成するために、本発明の化合物半導体装置では、化合物半導体基板の一主面上に形成された動作層と、この動作層上に設けられたゲート電極と、このゲート電極を挟んで前記動作層上で対向するソース電極及びドレイン電極と、前記化合物半導体基板の裏面に形成された導体層と、前記ソース又はドレイン電極と電気的に接続されかつバイアホールを通して前記裏面導体層と電気的に接続されたソースパッド部又はドレインパッド部と、前記化合物半導体基板と前記ソースパッド部又はドレインパッド部との間に配置され、前記化合物半導体基板を腐蝕するエッチング手段に耐蝕性を有する薄膜層とより成ることを特徴とする。

また、その製造方法は、この化合物半導体基板の一主面上にゲート電極と、このゲート電極を挟んで対向するソース電極及びドレイン電極とを形成する工程と、前記化合物半導体基板を腐蝕するエッチング手段に耐蝕性を有する薄膜を形成する工程と、前記薄膜上及び前記化合物半導体基板上に引出して設けられ、前記ソース又はドレイン電極と電気的に接続された各パッド部を形成する工程と、前記化合物半導体基板を裏面側からエッチングし、前記薄膜層に到達する貫通孔を形成する工程と、前記薄膜層をエッチングし前記ソース又はドレインパッド部に到達するバイアホールを形成する工程と、前記バイアホールを介して前記パッド部と電気的に接続された裏面導体層を形成する工程とを含むことを特徴とする。

また、化合物半導体基板がＩｎＰであることを実施態様とする。

（作用）

本発明によれば、ＩｎＰ基板を腐蝕するエッチング手段に耐蝕性を有する薄膜をソース（又はドレイン）パッド電極部と前記化合物半導体層との間に介在させるため、貫通孔形成工程において、ＩｎＰ基板上に形成されたソース（又はドレイン）パッド電極を腐食又は溶解させることなく、良好な形状のバイアホールを基板裏面から形成することが可能となり、バイアホール構造を有する高出力ＩｎＰ　ＦＥＴを提供することができるようになる。

（実施例）

以下、本発明における第１の発明の一実施例について、図面を参照して説明する。

第１図は第１の発明の一実施例の化合物半導体装置（ＩｎＰ絶縁ゲート型電界効果トランジスタ、以下ＩｎＰ　ＭＩＳＦＥＴと記す）の断面図である。第１図において、１０は半絶縁性ＩｎＰ基板で、その一方の主面上にクロライドＶＰＥ（Vapor Phase Epitaxial）法によりバッファ層１１，ｎ型動作層１２が順次形成されている。前記ｎ型動作層１２上にはAuGeで離間して形成されたソース電極１３Ｓ、ドレイン電極１３Ｄと、これら両電極に挟まれた領域にはゲート絶縁膜１３Ｉ、及びこのゲート絶縁膜上にゲート電極１３Ｇとが設けられている。ソース電極１３Ｓからはソース電極１３Ｓと電気的に接続されたソースパッド電極１４が引出して形成される。このパッド電極１４は、ＩｎＰ基板を腐蝕するエッチング手段に耐蝕性を示す薄膜１５（例えばSiO$_2$）上をバイアホール１６まで引出されており、このバイアホール１６を通して裏面金属層１７と電気的に接続されている。

次に、第２の発明のＩｎＰ　ＭＩＳＦＥＴの製造方法の一実施例について、工程順に示す断面図の第２図（ａ）～（ｄ）によって説明する。

まず、第２図（ａ）に示したように、半絶縁性ＩｎＰ基板１０の一方の主面上にクロライドＶＰＥ法によりバッファ層１１，ｎ型動作層１２を順次形成する。メサエッチングにより素子間分離を行なった後、ｎ型動作層１２上にAuGeによりソース電極１３Ｓ、ドレイン電極１３Ｄを形成し、これら両電極に挟まれたｎ型動作層１２の表面に絶

4S.13S. ソース電極
4D.13D. ドレイン電極
4G.13G. ゲート電極
5. 貫通孔
10. 半絶縁性InP基板
11. バッファ層
12. n型動作層
131. ゲート絶縁膜
14. ソースパッド電極
15. 薄膜
16a. InPの開孔
16b. 薄膜15の開孔
16. バイアホール
17. 裏面金属層
18. フォトレジスト
19. フォトレジストの開孔

代理人 弁理士 則近 憲佑
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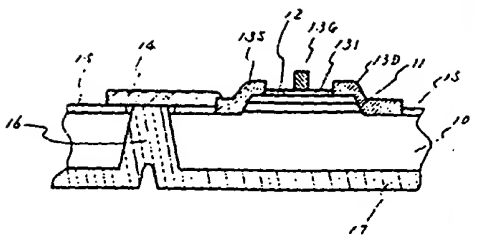
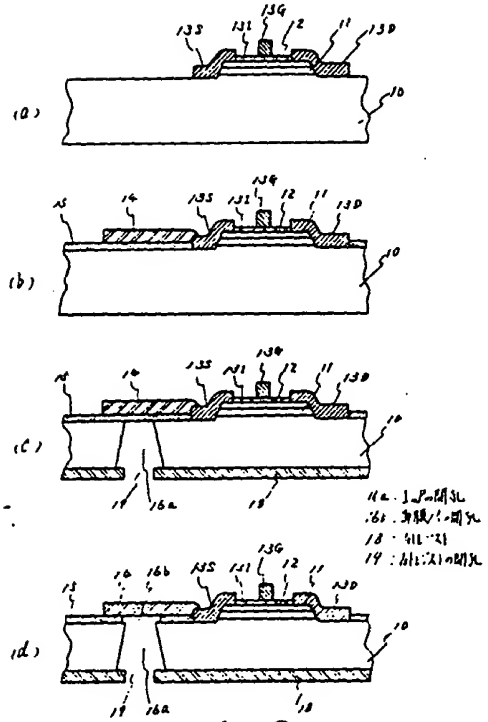


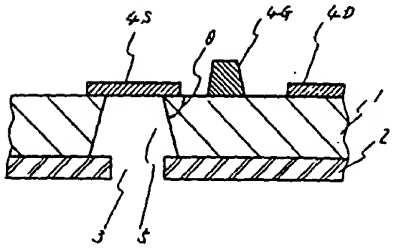
10 半絶縁性InP基板
11 バッファ層
12 n型動作層
131 ゲート絶縁膜
13G ゲート電極
13S ソース電極
13D ドレイン電極
14 ソースパッド電極
15 薄膜
16 バイアホール
17 裏面金属層

第1図



11a：InP開孔
131：薄膜15の開孔
18：フォトレジスト
19：フォトレジストの開孔

第2図



1 ： InP半導体基板
2 ： フォトレジスト等のエッチングマスク
3 ： マスクの開孔部
4G ： ゲート電極
4S ： ソース電極
4D ： ドレイン電極
5 ： 貫通孔

第3図

[Translation]

(19) Japan Patent Office
(12) **Patent Release (A)**

(11) Patent Application Release

Hei.4 (1992)-133472

(43) Release Date: May 7, 1992

(51) Int.Cl[5]	Identification No.	Agency Control No.
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		7353-M H 01 L 21/88 A
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Examination Request: Not yet requested
Items in Application: 3 (Total pages)

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(54) Name of Invention: Compound Semiconductor Device and Its Method of Manufacture

(21) Patent Requested: Hei.2(1990)-254310

(22) Date Requested: September 26, 1990

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Specifications

1. **Name f Invention:** Compound Semiconductor Device and its Method of Manufacture

2. Scope of Patent Application

(1) A compound semiconductor substrate consisting of

- an operating layer formed on one main surface of a compound semiconductor substrate,
- a gate electrode installed on this operating layer,
- source and drain electrodes bracketing and facing this gate electrode on this operating layer,
- a conductive layer formed on the back side of the above-noted compound semiconductor substrate,
- a source pad or drain pad connected electrically with th above-noted source and drain electrodes as well as with the above-noted rear-side conductive layer through a viahole, and
- a thin-film layer positioned between the above-noted compound semiconductor substrate and the above-noted source pad or drain pad and given corrosion resistance by etching that incises the above-noted compound semiconductor substrate.

(2) A method of fabricating a compound semiconductor device characterized by including

- a process forming a gate electrode and source and drain electrode facing and bracketing this gate electrode on one main surface of the compound semiconductor substrate,
- a process forming a thin film with corrosion resistance by etching which incises the above-noted semiconductor substrate,
- a process forming each pad that is installed extending from the above-noted thin film and semiconductor substrate and electrically connected to the above-noted source and drain electrodes,
- a process etching the semiconductor substrate from the rear side of the above-noted semiconductor substrate and forming a lead-through hole* that reaches through to the above-noted thin-film layer,
- a process etching the above-noted thin-film layer to form a viahole through to the above-noted source and drain pads, and
- process forming a rear-side conductive layer connected electrically to the above-noted pads through the above-noted viahole.

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* Translator's note: Original text uses term "lead-through hole" in Chinese characters and "viahole" in Japanese phonetics. Same thing? Also, original text not bulleted. Bullets added for readability.

(3) The method of fabricating the compound semiconductor device described in Application Item (2), which is characterized by the compound semiconductor substrate being InP.

3. Detailed Explanation of Invention

Purpose of Invention

Field for Commercial Utilization: This invention bears on a compound semiconductor device and its method of fabrication, and particularly applies to a field-effect transistor in which InP is used, and to its method of fabrication.

Usual Technology

Because its electron-saturation rate is high compared to GaAs, which currently is in the main stream of microwave semiconductor elements, and its thermal conductivity is high, InP is drawing attention as a material for power microwave semiconductor elements from which high frequencies and high output operation are obtained.

As one important technique for working out higher output and higher frequency for field-effect transistors (FET) for power, there is the technique of forming viaholes. What we call a viahole here indicates one which, when an FET equipped with source, drain and gate electrodes is formed, for instance, singly or severally on an InP substrate, is installed from the rear side of this substrate from the source (or drain) electrode or extending from the source (or drain) electrode, and a lead-through hole installed to reach to a source (or drain) pad electrode electrically connected to this source (or drain) electrode; and each source (or drain) electrode is electrically connected to a rear-side metallic layer made on the substrate's reverse side. By connecting the source electrode (or source pad electrode) through the viahole to the rear-side metallic layer one can electrically connect and ground each of the source electrodes without having to bond them to each matching source pad electrode. As one then can reduce grounding parasitic inductance from the bonding, high-frequency operation is made possible.

This viahole-forming technique is necessarily indispensable for making an InP FET high output and high frequency; but as yet no examples have been reported of having succeeded in making that for an InP FET. This is due to the following problems existing when forming viaholes through an InP substrate.

Figure 3 is a cross-sectional diagram explaining the usual viahole and its method of formation. In Figure 3, 1 is the InP semiconductor substrate, 2 is an etching mask for a photo-resist or the like, 3 is an opening made in this mask, 4S is a source (or source pad) electrode, 4D is a drain electrode, 4G is a gate electrode and 5 is the lead-through hole.

To form lead-through hole 5 shown in Figure 3 one uses such so-called dry etching as reactive-ion etching or such so-called wet etching as that with a solution. Generally, however, when etching InP by dry-etching, the etching has a small etching rate of 1μm/min or less; and no suitable material to serve adequately as a mask for this etching. Conversely, with the wet-etching method, etching solutions are known with high etching rates for InP, such as mixed solutions of HCl/H_3PO_4, $K_2Cr_3O_7/HBr/Ch_3COOH$ or $Br_2/HBr/H_2O$. Yet, because the usual mask of positive-type photo resist shows no tolerance for a mixed solution of HCl/H_3PO_4, metal masks, etc., must be used, making the processing complex. On top of that, there is the problem that its verticality is poor for the etching shape. (The θ shown in Figure 3 is 20~30°.)

With mixed solutions of $K_2Cr_2O_7/HBr/CH_3COOH$ or $Br_2/HBr/H_2O$ the photo resist has such resistance depending on the makeup, so that etching of relatively good verticality (θ shown in Figure 3 is 54-55°) can be done. However, these etching solutions readily corrode source (or drain) electrodes or source pad electrode areas (or drain pad electrode areas) made of such metals as AuGe in which gold is the main component. Due to this, when etching an InP substrate from its rear surface, there is the problem of the AuGe electrode disappearing if the substrate is even slightly over-etched, raising an obstacle to forming the kind of lead-through hole shown in Figure 3.

Problems the Invention Seeks to Resolve

As described above, making a lead-through hole by etching from the substrate's rear side for forming a viahole in the InP substrate--the commonly known method--is troublesome and has been a major obstacle to making InP FETs high output and high frequency.

This invention was devised to resolve the above-noted problems and has the purpose of providing an InP FET with good qualities equipped with a viahole structure, as well as its fabrication method.

Makeup of Invention

Means to Resolve Problems

For achieving the above purpose, this invention's compound semiconductor device has the characteristic of consisting of an operating layer formed on one main surface of a compound semiconductor substrate, a gate electrode installed on this operating layer, a source and drain electrode bracketing and facing the gate electrode on this operating layer, a conductive layer formed on the rear side of above-noted compound semiconductor substrate, a source pad or drain pad connect d electrically to the above-noted source and drain electrodes as well as to the above-noted rear-side conductive layer through a viahole, and a thin-film layer placed between th above-noted compound semiconductor substrate and the above-oted source pad or drain pad and given corrosion resistance by etching to incise the above-noted compound semiconductor substrate.

Also, its method of fabrication is characterized by including a process forming a gate electrode and source and drain electrode facing and bracketing this gate electrode on one main surface of the compound semiconductor substrate, a process forming a thin corrosion-resistant film by etching that incises the above-noted semiconductor substrate, a process forming each pad installed to extend out from the above-noted thin film and semiconductor substrate and be electrically connected to the above-noted source and drain electrodes, a process to etch the semiconductor substrat from the rear of the above-noted semiconductor substrate and form a lead-through hole reaching through to the above-not d thin-film layer, a process etching the above-noted thin-film layer to make a viahole through to the above-noted source and drain pads, and a process forming a rear-side conductive layer connected electrically to the above-noted pads through the above-noted viahole.

Again, it is effected in a format whereby the compound semiconductor substrate is InP.

Effects: With this invention, because a corrosion-resistant thin film is interposed between the source (or drain) pad electrode area and the above compound semiconductor layer as a means in the etching to incise the InP substrate, it becomes possible in the lead-through hole forming process to make a well-shaped viahole from the substrate's rear sid without corroding or dissolving the source (or drain) pad electrode formed on the InP substrate, and so is possibl to provide a high-output InP FET with a viahole structure.

Application Example: In the following we will explain an application example of this invention's first invention, referring to the figures.

Figure 1 is a cross-sectional diagram of the compound semiconductor device of one application example of the first invention (an InP insulating-gate type field-effect transistor, hereafter called an InP MISFET). In Figure 1, 10 is the semi-conductive InP substrate. On one side of its main surface, buffer layer 11 and n-type operating layer 12 have been formed sequentially by the chloride VPE (vapor phase epitaxial) method. Source electrode 13S and drain electrode 13D formed on above n-type operating layer 12 and separated by AuGe, as well as gate-insulating film 13I in the region flanked by these two electrodes and gate electrode 13G on this gate-insulating film are all installed. Source pad electrode 14, which is electrically connected to source electrode 13, is formed extending from source electrode 13S. This pad electrode 14 extends to viahole 16 on thin film 15 (of SiO_2 for instance) which exhibits corrosion resistance in the etching to incise the InP substrate; and it is connected electrically to rear-side metal layer 17 through this viahole 16.

Next, we will explain an application example of the second invention's method for fabricating an InP MISFET, using the cross-sectional diagrams of Figures 2(a)~(d) which show the processing sequence.

First, as shown in Fig. 2(a), we sequentially form buffer layer 11 and n-type operating layer 12 by chloride VPE on the main surface at one end of semi-insulating InP substrat 10. After using mesa-etching to effect element isolation, we form source electrode 13S and drain electrode 13D of AuGe on n-type operating layer 12, form insulating film 13I on the outer surface of n-type operating layer 12 bracketing these two electrodes, and form gate electrode 13G on this gate-insulating film. Next, after using CVD (chemical vapor deposition) to laminate SiO_2 film 15 200~500nm thick on a prescribed region, on SiO_2 film 15 we form source pad electrode 14 which is connected electrically to source electrode 13S and made of an Au/Pt/Ti laminated structure. (Figure 2[b]). All of the above processes are easily done by well-known methods.

Next, by wrapping and polishing the back side of this InP substrate 10's main surface one forms photo-resist layer 18 in a thin layer about 50μm thick applied to the rear side. After this, one forms opening 19 in photo-resist layer 18 so

as to site it directly under a prescribed position of source-pad electrode 14 on the substrate's outer surface. Then, using a mixed etching solution of $Br_2/HBr/H_2O$, one etches for three to five minutes to form hole 16a through SiO_2 film 15 as shown in Fig. 2(c). When doing this, the etching will stop at SiO_2 film 15, even if one over-etches somewhat, so that source pad electrode 14 will not be corroded.

Now, continuing from the etching of above-noted InP substrate, one etches SiO_2 film 15 in an ammonium fluoride solution to open up hole 16b in SiO_2 film 15 and form viahole 16. (Fig. 2[d]) Here, the AuGe will not be corroded by a little over-etching, as it has resistance to ammonium fluoride. Next, after discarding photo resist 18 used as an etching mask, one does gold-plating from the rear side to connect the rear-surface gold electrically to source pad electrode 14 through viahole 16 and so complete the InP MISFET equipped with a viahole as shown in Figure 1.

Above-noted thin film 15 need not be limited to silicon dioxide, but may also be such insulating film as SiN_x. Here the effects of this invention may even obtain with a conductive thin film exhibiting thin film 15's corrosion resistance to the etching medium incising the InP substrate. Nevertheless, with InP, since the adhesive power of a metal/semiconductor interface is generally weak compared to GaAs et al., such relatively adhesive metals as Ni, Ti, Al or Pd are easily corroded in etching solutions useable in making a viahole, such as $Br_2/HBr/H_2O$. So, these are not suitable as thin film 15. Also, even if a conductive (metal) film presumed suitable were to exhibit corrosion resistance to an etching medium, electrochemical reactions easily arise in this case with the etching solution at the thin film/InP interface, strongly inviting such undesirable effects as abnormal interface etching. For this reason, insulating film for thin film 15 such as in the application example is appropriate.

Again, the various electrode layers described above need not be limited to those of the above application example. For example, the source or drain electrodes may be metals making ohmic contact with n-type operating layer 12, or the metal may have a multi-layered structure as the bottom-most layer. Also, in the above application example we explained a case of applying this invention to an InP MISFET. Yet, the effects of this invention are not limited to this FET, but may apply also to an InP-junction type field-effect transistor. Also, it is clear from the above explanation that it

could be applied as well to compound semiconductor substrates other than InP.

Invention's Effectiveness: With this invention as described above, it is possible to provide a transistor, especially an InP FET and its fabrication method, equipped with a well-shaped viahole structure without dissolving or corroding the metal electrode layer installed on the outer surface of the semiconductor substrate when forming the viahole through to the outer surface from the rear surface of the compound semiconductor, particularly an InP semiconductor substrate.

4. Simple Explanation of Figures

Figure 1 is a cross-sectional diagram of an insulated-gate type field effect transistor illustrating one application example of this invention.

Figures 2(a)~(d) show, in its process sequence, the method of fabricating the insulated-gate field-effect transistor of one application example of this invention. All are cross-sectional diagrams.

Figure 3 is a cross-sectional diagram to explain the usual viahole.

1 ..... InP semiconductor substrate
2 ..... Etching mask, such as photo resist
3 ..... Hole-opening area of mask
4S, 13S .. Source electrode
4D, 13D .. Drain electrode
4G, 13G .. Gate electrode
5 ..... Lead-though hole
10 ..... Semi-insulating InP substrate
11 ..... Buffer layer
12 ..... n-type operating layer
13I ..... Gate-insulating film
14 ..... Source-pad electrode
15 ..... Thin film
16a ..... Opening in InP
16b ..... Opening in thin film 15
16 ..... Viahole
17 ..... Rear-surface metal layer
18 ..... Photo resist
19 ..... Photo resist's opening

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